# Yohann Uguen

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## Education

May 2019 — **ARCHI 2019**, *Summer school on embedded architectures and software*, Lorient, France.

March 2017 — **ARCHI 2017**, *Summer school on embedded architectures and software*, Nancy, France.

2014-2016 — **MSc. Student in Computer Science**, *École Normale Supérieure de Rennes / Université Rennes 1*, Rennes, France, Highly selective training; Major of promotion.

2013-2014 — **BSc. in Computer Science**, *Université Rennes 1*, Rennes, France.
Ranked: Third out of 83

2011-2013 — **BSc. in Mathematics**, *Université Rennes 1*, Rennes, France, Discontinued, switched majors to Computer Science.

2009-2011 — **Post-secondary preparatory school**, *Sainte-Anne*, Brest, France, Classes preparing for entrance examinations to the French Grandes Ecoles.

2009 — **High School Diploma**, *(Major: Mathematics), Lycée Brizeux*, Quimper, France.

## Experience

January 2020 - Today — **FPGA software engineer**, *Intel*, London, United Kingdom.
Working on the Intel HLS/OpenCL/DSP Builder backend on arithmetic and compiler optimizations.

Septembre 2016 - December 2019 — **PhD student in computer science (graduated)**, *CITI Lab - INSA Lyon*, Villeurbanne, France.
***Thesis topic***: Arithmetic optimizations for high-level synthesis. This thesis aims at improving the quality of the electronic circuits generated by high-level synthesis tools by applying arithmetic optimizations. These optimizations are either:
- existing ones from classical conception flows. The goal is then to extend these optimizations using compiler knowledge given by high-level synthesis tools. Then, to generate corresponding compiler optimizations.
- yet to be discovered using this new vison of a circuit (a program).

Septembre 2016 - September 2019 — **Teaching assistant**, *INSA Lyon*, Villeurbanne, France.
Being integrated to the computer science teaching team at INSA Lyon, I have to create and/or give courses around the following subjects:
- *Introduction to Linux*; Command line, file system, file system permissions, etc.
- *Digital circuits architecture*; Boolean algebra, combinatory logic, Logisim
- *Computer architecture*; Von Neumann architecture, automatons encoding, creation of a simplified processor
- *Operating systems* ; Threads, parallelism, synchronization
- *Compilation* ; Creation of a compiler for a subset of C in C, Yacc, Bison

May - August 2018 — **Invited researcher**, *Intel*, Paris, France.
The goal of this collaboration was to run Python code on a Programmable Acceleration Card (PAC) with Arria 10 GX FPGA. As there was no High-Level Synthesis (HLS) tool from Python, we used the following methodology:
- *Retrieve LLVM IR from Python*: Using Numba
- *Integrate this IR in OpenCL to FPGA HLS flow*: Generate C code, Perl scripts, Python scripts
- *Retrieve the computed result in Python*

February - July 2016 — **Intern**, *CITI Lab - INSA Lyon*, Villeurbanne, France.
***Internship topic***: Create plug-ins in a source-to-source tool (GeCoS) in order to apply code transformations for high-level synthesis tools (HLS). These transformations implement arithmetic optimizations over floating-point operators which are not supported by HLS tools. Such optimized operators are based on the ones from FloPoCo, a generator for optimized floating-point operators. Skills demonstrated:
- Compiler knowledge: Transformations on the GeCoS internal representation
- High-Level Synthesis tools : Programming for Vivado HLS
- Programming languages: *C/C++*, *Java*

May - August 2015 — **Short term scholar**, *Colorado State University*, Fort Collins, Colorado, USA.
I was working within the High Performance Computing team, called MELANGE.
***Internship topic***: Develop a cycle-accurate simulator for a parallel programmable architecture called the Stencil Processing Unit (SPU). The SPU was proposed as an energy-efficient architecture to implement a richer class of programs that can be handled by GPUs (Graphics Processing Unit)
Skills demonstrated:
- Ability to join an advanced project: Implementing the extensions in *gpgpu-sim*, a GPU simulator that provides precise information about architectural details and energy consumption
- Using the NVIDIA toolkit: Writing *CUDA* kernels and *PTX* assembly files
- Research thinking: Extending the *PTX ISA*, and the *gpgpu-sim* run time execution in order to overcome the theoretical problems faced
- Programming using different languages: *C++*, *Bison*, *Flex*, *Bash scripting*, *CUDA*, *PTX*

May - July 2014 **Intern**, *INRIA*, Rennes, France.

INRIA is a French national research institution focusing on Computer Science and Applied Mathematics.
***Internship topic***: Build a VLIW processor based on the Vex/ST200 using High-Level Synthesis tools
Skills demonstrated:

- Programming in *C* language: Writing a *VLIW* simulator in *C*
- High Level Synthesis (*HLS*) Tools: Using *HLS* tools to create hardware from *C*
- Programming in *Java* language: Writing an assembly in *Java*
- Usage of Computer Aided Design (*CAD*): Using *CAD* to run the *VLIW* on a Field Programmable Gate Array (*FPGA*)
- Team work: Working alongside a PhD. student that intends to use the *VLIW*
- Documentation: Writing a manual to record and provide support for the above processes

July 2012 - January 2016 **Tutor in Mathematics and Computer Science**, *for high school and college-level students*, Rennes, France.

Skills demonstrated:

- Pedagogy: Students grades improved (e.g. student went from 8/20 to 14/20)
- Organisation: Effectively managing six students in addition to my workload
- English: Teaching some courses, particularly in Computer Science, in English

## Languages

French Native

English Good speaking and writing skills

## Invited talks

October 2017 **RAIM 2017**, *French institutional meeting about arithmetic*, ENS Lyon, France.

June 2018 **Computation day at LIP on FPGAs**, *An introduction to FPGAs and how to program them*, LIP Lyon, France.

## Reviews

**As a sub-reviewer**, *FCCM 2017-2019; FPT 2017; DATE 2018,2020-2021*.

**As a reviewer**, *ICECS 2018; TCAS-II 2020*.

## References


Yohann Uguen, Florent De Dinechin, Victor Lezaud, and Steven Derrien. "Application-specific arithmetic in high-level synthesis tools". In: *ACM Transactions on Architecture and Code Optimization* (Mar. 2020). DOI: 10.1145/3377403. URL: https://hal.archives-ouvertes.fr/hal-02423363.

Florent de Dinechin, Luc Forget, Jean-Michel Muller, and Yohann Uguen. "Posits: the good, the bad and the ugly". In: *CoNGA'19 - Conference for Next Generation Arithmetic*. Singapore, Singapore: ACM Press, Mar. 2019, pp. 1–10.

Luc Forget, Yohann Uguen, and Florent De Dinechin. "Hardware cost evaluation of the posit number system". In: *Compas'2019 - Conférence d'informatique en Parallélisme, Architecture et Système*. Anglet, France, June 2019, pp. 1–7.

Luc Forget, Yohann Uguen, Florent de Dinechin, and David Thomas. "A type-safe arbitrary precision arithmetic portability layer for HLS tools". In: *HEART 2019 - International Symposium on Highly Efficient Accelerators and Reconfigurable Technologies*. Nagasaki, Japan, June 2019, pp. 1–6.

Yohann Uguen, Luc Forget, and Florent de Dinechin. "Evaluating the hardware cost of the posit number system". In: *29th International Conference on Field-Programmable Logic and Applications (FPL)*. IEEE. Barcelona, Spain, 2019, pp. 1–8.

Yohann Uguen and Eric Petit. "PyGA: a Python to FPGA compiler prototype". In: *AI-SEPS 2018 - 5th ACM SIGPLAN International Workshop on Artificial Intelligence and Empirical Methods for Software Engineering and Parallel Computing Systems*. Boston, United States: ACM, Nov. 2018, pp. 11–15.

Yohann Uguen and Florent de Dinechin. "Design-space exploration for the Kulisch accumulator ". working paper or preprint. Mar. 2017.

Yohann Uguen and Florent de Dinechin. "Exploration architecturale de l'accumulateur de Kulisch". In: *Compas'2017 - Conférence d'informatique en Parallélisme, Architecture et Système*. Sophia Antipolis, France, June 2017, pp. 1–8.

Yohann Uguen, Florent de Dinechin, and Steven Derrien. "A high-level synthesis approach optimizing accumulations in floating-point programs using custom formats and operators". In: *2017 IEEE 25th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*. Napa, United States: IEEE, Apr. 2017, pp. 80–80.

Yohann Uguen, Florent de Dinechin, and Steven Derrien. "Bridging High-Level Synthesis and Application-Specific Arithmetic: The Case Study of Floating-Point Summations". In: *27th International Conference on Field-Programmable Logic and Applications (FPL)*. IEEE. Gent, Belgium, Sept. 2017, p. 8.

Yohann Uguen, Florent de Dinechin, and Steven Derrien. *High-level synthesis and arithmetic optimizations*. Compas'2016. Poster. Lorient, France, July 2016.